Application. No. 09/687,897

IN THE CLAIMS

1. (Cancelled)

2. (Previously Presented) A method of selecting a signal among N signals, the selection taking place in that a validation signal associated with the signal to be selected is placed in an active state by means of a selection signal, which method comprises a reset step in which those validation signals which have not presented an active front since a given moment in time are reset to an inactive state, which reset step is carried out when at least two validation signals are simultaneously in an active state.

3 (Previously Presented) A method of selecting a signal among N signals, the selection taking place in that a validation signal associated with the signal to be selected is placed in an active state by means of a selection signal, which method includes a reset step in which all validation signals which have not presented an active front since a given moment in time are reset to an inactive state, which reset step is carried out when one of the validation signals presents an active front.

4. (Currently Amended) ~~The method of claim 1~~, **A method of selecting a signal among N signals, the selection taking place in that a validation signal associated with the signal to be selected is placed in an active state by means of a selection signal, which method includes an attribution step in which the state of the associated selection signal is attributed to each of the validation signals, which attribution step is carried out responsive to all the validation signals being in an inactive state** further comprising a reset step in which all validation signals which have

not presented an active front since a given moment in time are reset to an inactive state, which reset step is carried out when one of the validation signals presents an active front.

5. (Previously Presented) The method as claimed in claim 4, wherein the signal selected from among the N signals is a clock signal; and wherein the clock signal is supplied from a machine to a chip card, thereby enabling data to be exchanged between the chip card and the machine.

6. (Previously Presented) A switching device designed to deliver at an output a signal selected among N input signals when a validation signal associated with said input signal has been placed in an active state by means of an associated selection signal, which device includes:

attribution means capable of attributing to each of the validation signals the state of its associated selection signal, which means are intended to be activated when all the validation signals are in an inactive state, and

reset means capable of resetting to an inactive state those of the validation signals which have not presented an active front since a given moment in time, which means are intended to be activated when at least two validation signals simultaneously have an active state.

7. (Previously Presented) The switching device as claimed in claim 6, wherein it comprises in addition:

detection means for detecting active fronts of the selection signals, and

memory means for storing the state of the selection signals, which means are intended to be activated by the active fronts of said signals and to deliver the validation signals.

8. (Previously Presented) The switching device as claimed in claim 7, wherein it comprises in addition:

detection means for detecting that all the validation signals are simultaneously inactive, which detection means are intended to control the attribution means.

9.(Previously Presented) The switching device as claimed in claim 7, wherein it comprises in addition:

detection means for detecting fronts of the validation signals, which detection means are intended to control the reset means.

10. (Previously Presented) The switching device as claimed in claim 6, wherein the switching device is incorporated in an apparatus adapted to exchange data with a smart card, and is further adapted to supply to the smart card a clock signal selected from among N clock signals.

11. (Previously Presented) The switching device of Claim 8, wherein the detection means for detecting that all the validation signals are simultaneously inactive comprises a delay cell.

12. (Previously Presented) The switching device of Claim 9, wherein the detection means for detecting fronts of the validation signals comprises a delay cell.